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DESIGN OF A RECONFIGURABLE PIPELINED ARCHITECTURE FOR SRC FILTER FOR SOFTWARE RADIO RECEIVER

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ABSTRACT

In the receiver architecture of Software Defined Radio (SDR) channelization and sample rate conversion (SRC) are the two computational intensive tasks. CIC filters can be employed to achieve sample rate changes by integral factors but needs a gain compensation filter and fractional rate SRC to achieve the required sample rate. In this paper a pipelined architecture for the SRC employing joint compensation and interpolation, discrete compensation and interpolation method is simulated in Xilinx ISE 14.7 and implemented on KINTEX-7 XC7K325t-2FFG900 FPGA. The design is tested for four standards, viz., GSM900, CDMA2000, WCDMA and HiperLAN using Virtual Input Output Cores and Integrated Logic analyzers on Kintex-7 board. Comparison of two methods show that discrete compensation and interpolation outperforms when compared with joint compensation and interpolation technique at the cost of increased latency.

KEYWORDS: CIC Filter, DDC, Farrow Structure, Fpgas, IF, Interpolation, Symbol Rate, RF, SRC

INTRODUCTION

Mitola's architecture for ideal software defined radio encourages RF signal processing to be performed in digital domain [1]. It is due to the placement of analog to digital converter immediately after the antenna. However, this could not be reached in real time due to the limitations posed by the tighter specifications of ADCs [2], [3], [4]. Due to technological evolution and pipelined architectures for ADCs, viability of high sample rate ADCs may lead the path to ideal SDR. However, a sample rate converter is required to carry out signal processing tasks at baseband sample rate rather than at RF sampling rate so that power dissipation can be reduced in wireless devices. Synchronization of system parameters at the receiving end of a communication system according to the specifications of wireless standard is another aspect for a radio communication system [5]. Therefore a reconfigurable digital down converter is required for SDR application.

Today's SDR architecture is broadly divided into three stages viz., RF processing stage, Intermediate Frequency stage and baseband processing stage [6]. The intermediate frequency is chosen to be very large such that it can accommodate various wireless standards. In this stage the process of channelization and sample rate conversion takes place. Architecture for sample rate conversion is proposed in this paper. The down conversion factor may range from very high to very low based on the wireless standard. Therefore, reconfigurable Cascaded-Integrator-Comb (CIC) filters are employed to achieve the sampling rate change by a large factor [7]. CIC filters are implemented based on the method of factorization to reduce the complexity involved in their realization [6].

For integral SRCs CIC filters are the best candidates. CIC filters also suffers from the disadvantage that they have inherent gain droop in the pass band of the filter. Hence a compensation filter has to be employed for compensating gain

droop. Then the sample rate has to be altered by required fraction to meet the specifications of the standard. A joint compensation and interpolation filter based on Farrow structure has been proposed using frequency domain polynomials. The coefficients of the Farrow filter are computed such that the error is minimized in the least squares error sense or mini-max error sense [6]- [8].

In this paper, two architectures are implemented for sample rate conversions. Firstly, a joint compensation and interpolation method and secondly, the gain compensation filter and interpolation filter using Lagrange's interpolation polynomial is implemented. In the first method, the filter coefficients are computed by approximating the desired frequency response with a second order polynomial and coefficients are computed such that the error is minimized. In the second method, gain compensation filter for various standards are designed using inverse sinc low pass filters. The compensation filter coefficients are calculated using equiripple method and stored as a look up table. A method based on Taylor's series for interpolation has been proposed in [5], where the order of interpolation can be switched on the fly. However, the filter proposed in [5] shows the past sample f (t) depends on the future sample f (k) and f (k − 1). Therefore the output of the compensation filter is interpolated using Lagrange's interpolating polynomial of different orders and their responses are compared. The architecture is implemented in such a way that it can be easily reconfigured to extract the required signal of interest of any wireless standard with required symbol rate and spectral characteristics.

SAMPLE RATE CONVERTER

Sample rate conversion factor for software defined radio ranges from a high factor of 400 to a low factor of 4. Different architectures such as a low pass filter followed by a decimator/interpolator or half band filters may be employed for interpolation or decimation. However, the computation complexity of such an implementation is very high which is of the order of hundreds of millions multiplications per second. Hence the architecture for sample rate conversion for decimation is divided into three stages, namely, CIC filtering stage, Compensation and interpolation stage and half band filtering stage.

CIC Filter

CIC filters are first proposed by Hoganeur [7]. CIC filters are deployed when sample rate changes by large factors are required. These filters do not employ multipliers in their realization. An N^{th} order CIC filter for decimation employs 'N' integrators followed by a decimator and 'N' comb filters. Apart from their multiplier less architecture, rate change factor the only parameter which alters the characteristics of the filter and produces samples with new sampling rate. Thus CIC filters can be reconfigured with greater flexibility and ease as all its coefficients are unity.

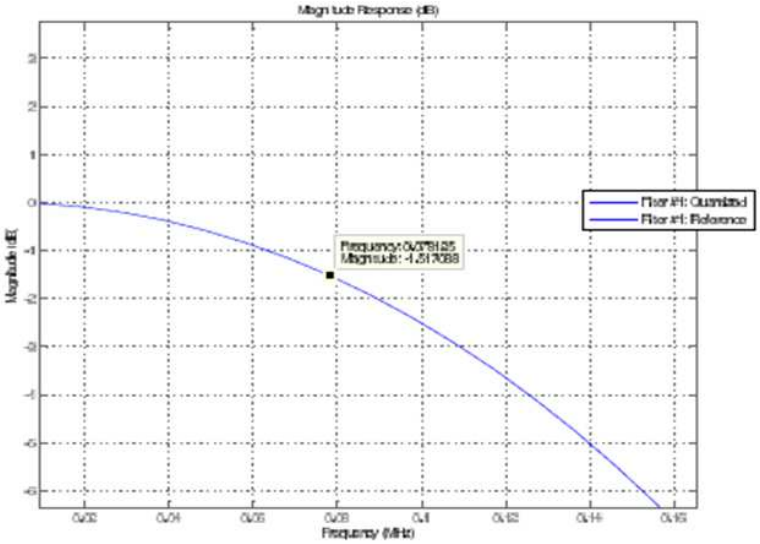

Figure 1: Frequency Response of Cascaded Integrator Decimation Filter with R=384

The transfer function of the filter is given as			
H(z) =	$(1 - z^{-RM})^N$ / $(1 - z^{-1})^N$		(1)
Where, R = Decimation Factor, M = Differential delay (1 or 2), N = No of Integrators/Combs			
If $z = e^{j\omega}$ then			
$H(j\omega) = R^N M^N * \sin(\omega)/\omega$			(2)

From the transfer function of CIC filter it can be inferred that the filter has a gain of $(RM)^N$. The number of bits required to realize the filter is directly proportional to the product of rate change and order of filter, which is a serious drawback for this filter. Number of bits in the implementation of CIC filter can be optimized by optimally choosing the order of the CIC filter and rate change factors. A factorization method for sample rate change is proposed in [6], [9] which reduces the bit growth rate and also the performance characteristics of the filter is improved. The CIC filters in are implemented with a rate change factor ranging from 2 to 8 with an order of 3 in three stages [9]. Thus the bit growth is of nine bits in each stage. Further, the number of bits within the CIC stages can also be optimized as stated in [10].

Secondly, frequency response of the filter is a sinc function as shown in Figure 1. A gain droop in the pass band of the filter has to be restored; hence a gain compensation filter has to be employed.

Compensation and Interpolation Filter

A compensation filter is needed to restore the gain in the pass band of the CIC filter. An interpolation filter, where the sampling rate of the signal has to be changed by a factor 'I', where $1 \leq I \leq 2$ is employed to achieve the symbol rate of the standard.

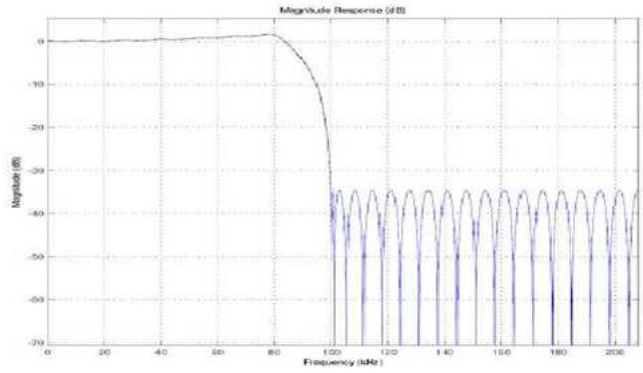

Figure 2: Frequency Response of Compensation Filter for GSM Standard

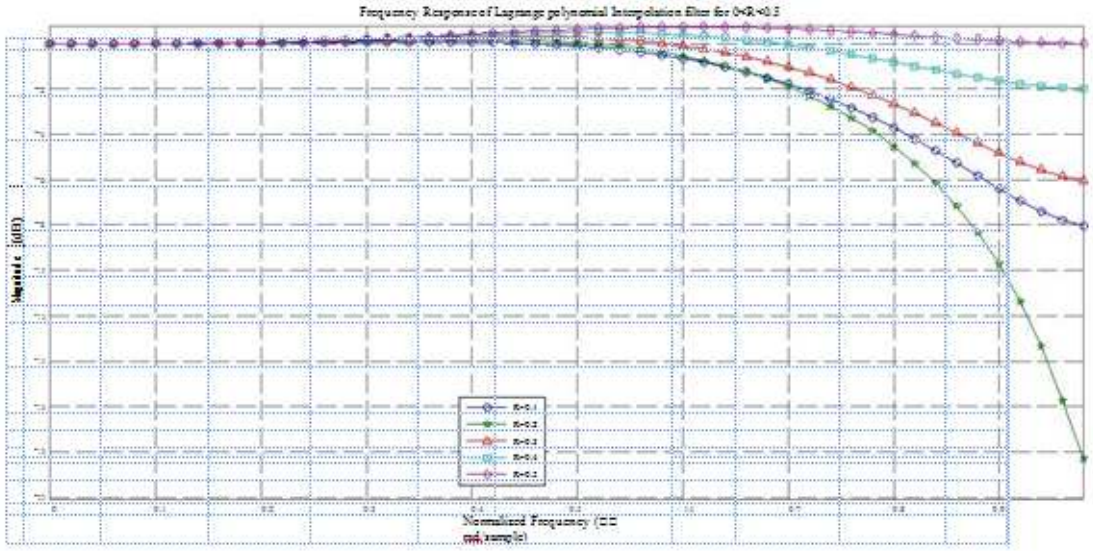

Figure 3: Frequency Response of Lagrange Interpolation Filter for Fractional Rate $0 \leq R \leq 0.5$

A scheme of joint compensation and interpolation based on frequency domain polynomials is proposed in [6]. In this method, the desired frequency response of the filter is approximated as a piecewise quadratic polynomial and implemented as a Farrow structure [8] [11], [12]. For a multi-standard software radio receiver the coefficients of the Farrow filter can be stored as a look up table and then interpolated by the required rate. Frequency response of joint compensation and interpolation method is found to be less accurate when the ratio F_p/F_s becomes higher.

The characteristics of compensation filter follow an inverse sinc response in the pass band of the standard. The coefficients of these filters are computed using FIR equiripple filter design method in MATLAB. The coefficients of the inverse sinc filter are provided based on the standard which is stored in a look up table. A fractional rate interpolation filter can be designed using various methods. In conventional method, fractional interpolation by a

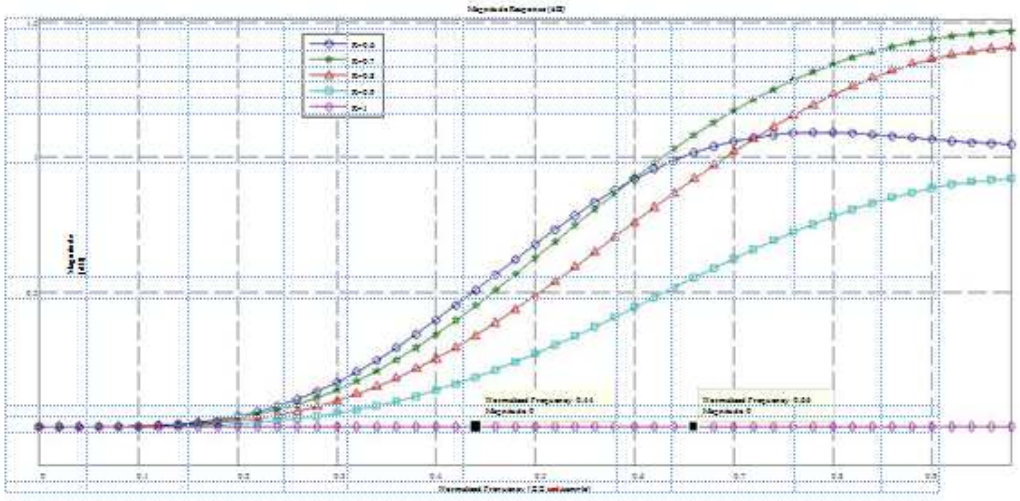

Figure 4: Frequency Response of Lagrange Interpolation Filter for Fractional Rate 0.6 ≤ R ≤ 1

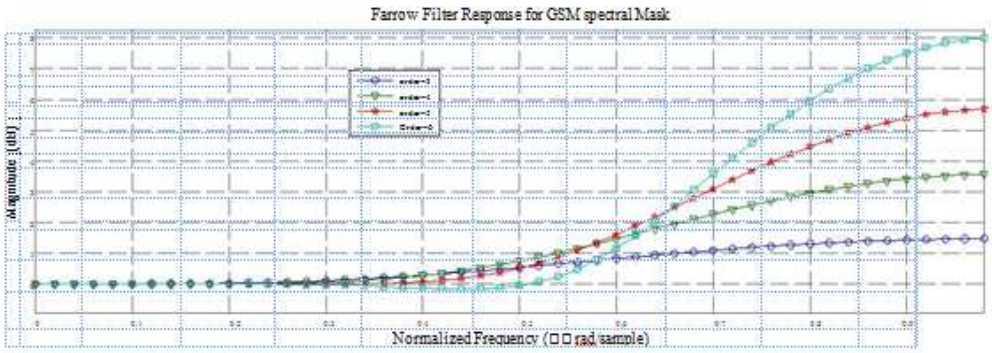

Figure 5: Frequency Response of Lagrange Interpolation Filter with Various Orders

factor of m/n can be achieved by first interpolating the sample rate by a factor 'm' and then decimating by a factor of 'n'. The method employs an anti-aliasing low pass filter to suppress the image components of the signal. In this method, the coefficients of low pass filter changes with change in fraction. Hence the method is less flexible. C.W. Farrow has proposed a polyphase structure where the change in the sampling rate is attained just by varying the value of digital delay element, coefficients of the polyphase filter remaining constant [12]. C.Candan has proposed a structure for interpolation based on Taylor series [5] and Newton's backward difference formula [13]. Though these architectures are recursive in design and have computational complexity of order O (N), they are not suited for FPGA implementation due to non-casual filter characteristics. Large SRC factors are unfavorable to these structures. The response of these structures can be improved only by increasing the order of the filter [13].

Lagrange's polynomial interpolation is proposed to interpolate the sample rate with the required rate. The order of the filter cannot be changed flexibly when compared with the Newton's structures as the coefficients of the polyphase structure vary with the order of the filter. The computational complexity of Farrow structure is of the order of O (N^2). However, the desired frequency response can be attained by selecting a relatively lower order filter when compared with Newton's structures. Thus the computational complexity is reduced.

The method for calculation of Lagrange's interpolation polynomial is presented in [14]. Figure 3 and 4 shows that as the fractional interpolation rate decreases the Lagrange interpolation filter behaves as a low pass filter with a flat pass band whereas the same is not true for higher fractional interpolation rates.

Figure 5 shows that the frequency response of Lagrange interpolation with α = 0.769 for various orders. The filter has a flat response in low frequency region whereas in high frequency region gain of the filter increases with increase in frequency.

RESULTS

SRC filter architecture employing joint compensation and interpolation, discrete compensation and Lagrange interpolation is implemented. Rate change factor is the reconfigurable parameter which selects the set of filter coefficients to attain the required spectral characteristics as shown in Figure 6.

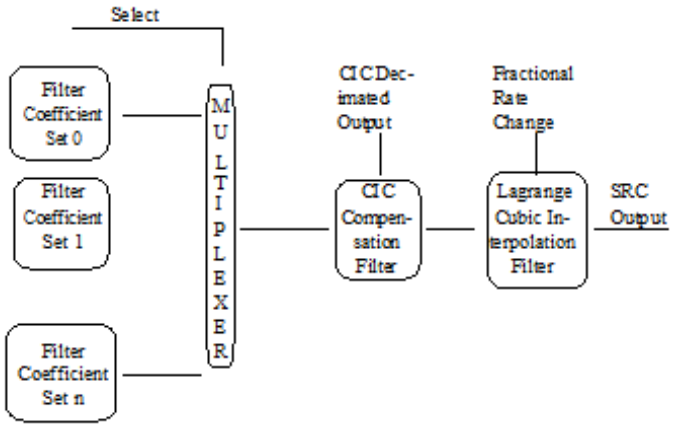

Figure 6: Proposed Architecture for Compensation and Interpolation for Multistandard Radio Receiver

The performance characteristics of the two methods are tabulated in Table 1. It can be inferred that though the joint compensation and interpolation has a low latency in comparison to discrete compensation and interpolation method, the former SRC filter has poorer pass band characteristics when compared with the later method.

Table 1: Performance Comparison of Joint Compensation and Interpolation Method(I) with Discrete Compensation Lagrange's Interpolation Method(II)

Radio Standard	Method I				Method II			
	δ_P	δ_S	Latency	Latency	δ_P	δ_S	Latency	Latency
	In Db	In Db	In CC	In µs	In Db	In Db	In CC	In µs
HiperLAN	0.8	17	400	2.5	0.05	18	800	5
WCDMA	0.45	18	1626	10.16	0.1	34	2584	16.15
CDMA2000	0.05	19	3646	22.78	0.07	18	7813	48.83
GSM900	0.46	3	11816	73.85	0.1	19	37810	236.31

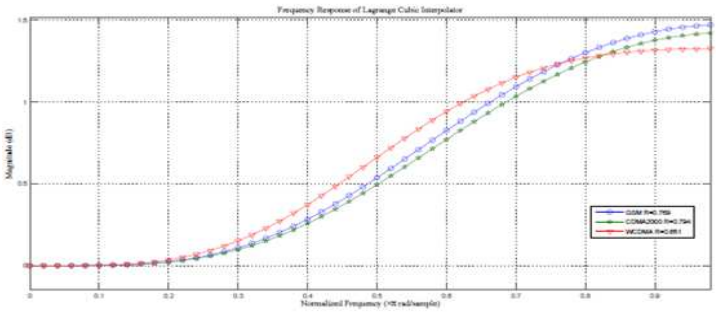

Figure 7: Frequency Response of Lagrange Interpolation Filter for GSM, CDMA, WDCDMA

From the frequency response of the Lagrange polynomial filter it is observed that as the order of the filter increases, the gain in the high frequency region increases as shown in Figure 5. Hence we choose Lagrange Cubic polynomial interpolation to interpolate the signal samples to meet the symbol rate of the standard. Figure 7 shows the response of the Lagrange cubic interpolation filter for GSM900, CDMA2000, WCDMA where the gain of the filter is less than 1.5dB even in the high frequency range.

Table 2: Comparison of Hardware Resource Utilization for Joint Compensation and Interpolation Method with Lagrange's Interpolation Method on Kintex-7 FPGA

Hardware Resources	Method I	Method II
Slice Registers	28371	24452
Slice LUTs	48222	44724
LUT-FF Pairs	21531	17969
Frequency(MHz)	355	355

Architectures for joint compensation and interpolation, CIC compensation and Lagrange interpolation is simulated using Xilinx ISE 14.7 design suite and implemented on Xilinx XC7K325t-2FF900 FPGA. Coefficients of the filter are computed to attain passband ripple of 0.1dB. However, from Table 1 it can be inferred that method I has a deviation in filter characteristics with highest passband ripple of 0.8dB for HiperLAN standard whereas the passband ripple in method II does not exceed 0.1dB for any of the radio standards. The implemented architecture is tested with an input clock frequency of 160MHz. Latency comparison of both methods shows that the latency of method I is reduced by more than fifty percent in comparison to method II (Table 1). From table 2, it can be inferred that hardware resource utilization for method I is about 15 percent higher in comparison to method II.

CONCLUSIONS

A reconfigurable architecture for sample rate conversion is proposed. A sampling rate converter employing CIC filter, CIC compensation filter and interpolator is implemented on FPGA. Among the filters employed, CIC filters can be reconfigured by providing an integer decimation rate, interpolator is reconfigured by providing the required fractional delay parameter based on the standard. Hence, a CIC compensation filter with required spectral characteristics based on Look-up table method is employed to restore the gain droop in the pass band of the required standard. The implemented filter architecture has good filter characteristics and requires lesser hardware resources in comparison to joint compensation and interpolation method at the cost of increased latency. Design of low latency SRC filter architecture can be the future scope of this work.

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